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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/071,072	02/08/2002	Samuel Naffziger	10016631-1	3388

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HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
MCCARTHY, CHRISTOPHER S	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 04/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/071,072	NAFFZIGER, SAMUEL	
	Examiner	Art Unit	
	Christopher S. McCarthy	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: The title misspells the word "manufacturing". Appropriate correction is required.

Claim Objections

2. Claims 8-10 are objected to under 37 CFR 1.75 as being a substantial duplicate of claims 14-16. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-11, 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robbins et al. U.S. Patent 6,067,633 in view of Henry et al. U.S. Patent 5,889,679.

As per claim 8, Robbins teaches a method of selling a partially defective processor integrated circuit comprising the steps of: providing a plurality of functional units on the integrated circuit (column 2, lines 20-25); wherein the functional units of the plurality of functional units may be marked with status selected from the group consisting of enabled and disabled (column 3, lines 29-31; column 5, lines 55-65); testing an integrated circuit to determine which functional units are defective (column 2, lines 20-42); mark defective functional units as disabled and remaining functional units as enabled (column 5, lines 55-65); classifying the integrated circuit into bins according to performance available with the enabled functional units; packaging the integrated circuit; and selling the integrated circuit as capable of performance appropriate for the bin into which it was classified (column 3, lines 44-57). Robbins does not explicitly teach providing a resource status register and programming the resource status register according to the status of the functional units; however, Robbins does teach using a control logic control circuit to impose status bits to the functional units. Henry does teach providing a resource status register and programming the resource status register according to the status of the functional units (column 4, lines 47-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register of Henry in the control logic circuit of Robbins. One of ordinary skill in the art would have been motivated to use the register of Henry in the control logic circuit of Robbins because Henry teaches using the register as a feature control register which configures the functional blocks as enabled or disabled; an explicit desire taught by Robbins (column 5, lines 29-31).

As per claim 9, Robbins teaches the method of claim 8, wherein the step of classifying is performed by a table lookup, the table having been prepared based upon benchmark results

(column 3, lines 44-57, wherein, Robbins teaches the unit's functionality as based upon the standards set by the manufacturer).

As per claim 10, Robbins teaches the method of claim 8, wherein the functional units include a plurality of integer execution units and a plurality of floating point execution units (column 1, lines 7-10, wherein, an integer execution unit (ALU) and a floating point execution unit is inherent in each processing unit of the multiprocessing unit chip).

As per claim 11, Robbins teaches the method of claim 10, wherein at least one defective floating point unit of the plurality of floating point execution units is marked disabled and at least one remaining floating point unit of the plurality of floating point execution units is marked enabled (column 5, lines 29-31).

As per claim 14, Robbins teaches a method of selling a partially defective processor integrated circuit comprising the steps of: providing a plurality of functional units on the integrated circuit (column 2, lines 20-25); wherein the functional units of the plurality of functional units may be marked with status selected from the group consisting of enabled and disabled (column 5, lines 55-65); testing an integrated circuit to determine which functional units are defective (column 2, lines 20-42); mark defective functional units as disabled and remaining functional units as enabled (column 5, lines 55-65); classifying the integrated circuit into bins according to performance available with the enabled functional units; packaging the integrated circuit; and selling the integrated circuit as capable of performance appropriate for the bin into which it was classified (column 3, lines 44-57). Robbins does not explicitly teach providing a resource status register and programming the resource status register according to the status of the functional units; however, Robbins does teach using a control logic control circuit to impose

status bits to the functional units. Henry does teach providing a resource status register and programming the resource status register according to the status of the functional units (column 4, lines 47-49). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register of Henry in the control logic circuit of Robbins. One of ordinary skill in the art would have been motivated to use the register of Henry in the control logic circuit of Robbins because Henry teaches using the register as a feature control register which configures the functional blocks as enabled or disabled; an explicit desire taught by Robbins (column 5, lines 29-31).

As per claim 15, Robbins teaches the method of claim 14, wherein the step of classifying is performed by a table lookup, the table having been prepared based upon benchmark results (column 3, lines 44-57, wherein, Robbins teaches the unit's functionality as based upon the standards set by the manufacturer).

As per claim 16, Robbins teaches the method of claim 14, wherein the functional units include a plurality of integer execution units and a plurality of floating point execution units (column 1, lines 7-10, wherein, an integer execution unit (ALU) and a floating point execution unit is inherent in each processing unit of the multiprocessing unit chip).

As per claim 17, Robbins teaches the method of claim 14. Robbins does not teach wherein the resource status bits are set according to results of built in self test upon powerup of each functional unit. Henry does teach wherein the resource status bits are set according to results of built in self test upon powerup of each functional unit (column 4, lines 57-65). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the BIST of Henry in the manufacturing process of Robbins. One of ordinary skill in the art

would have been motivated to use the BIST of Henry in the manufacturing process of Robbins because Henry teaches the reading of the register status bits as to provide the modification needed after the unit has been powered; this is an explicit desire of Robbins in the testing of the unit in the initial stages of development (column 8, lines 54-64).

5. Claims 12-13, 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Robbins in view of Henry in further view of *Microsoft Computer Dictionary*.

As per claim 12, Robbins and Henry teach the method of claim 8, wherein a functional unit of the plurality of functional units is capable of being disabled through programming the resource status bits (column 5, lines 29-31 and as argued in claim 11 above). Robbins and Henry do not explicitly teach wherein in the functional unit is a branch prediction unit. *Microsoft Computer Dictionary* does teach wherein a functional unit of processor unit can consist of a branch prediction unit (page 60). It would have been obvious to one of ordinary skill in the art at the time the invention was made to utilize a branch prediction unit in the processor unit of Robbins. One of ordinary skill in the art would have been motivated to utilize a branch prediction unit in the processor unit of Robbins because a benefit of using a branch prediction unit, as taught by *Microsoft Computer Dictionary,* is to prevent a pipeline break in the processor so as to not slow down the system as a whole. If the branch prediction unit is, therefore, disabled or broken, as taught by *Microsoft Computer Dictionary,* then the processor will be slower and will not be sellable as a top-line processor and will have to be sold at a lower performance level; a desire explicitly taught by Robbins (column 5, lines 55-65).

As per claim 13, Robbins teaches the method of claim 12, wherein at least one defective floating point unit of the plurality of floating point execution units is marked disabled and at least one remaining floating point unit of the plurality of floating point execution units is marked enabled (column 5, lines 29-31).

As per claim 18, Robbins teaches the method of Claim 14. Robbins does not teach wherein the resource status bits are implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale. Henry does teach wherein the resource status bits are implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale (column 4, lines 47-49; column 6, lines 30-34). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register programming of Henry in the control logic circuit of Robbins. One of ordinary skill in the art would have been motivated to use the register programming of Henry in the control logic circuit of Robbins because Henry teaches using the register as a feature control register which configures the functional blocks as enabled or disabled and programming so before shipping; an explicit desire taught by Robbins (column 5, lines 29-31; column 3, lines 44-57).

As per claim 19, Robbins teaches the method of Claim 11. Robbins does not teach wherein the resource status bits are implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale. Henry does teach wherein the resource status bits are implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale (column 4, lines 47-49; column 6, lines 30-34). It would have been obvious to one of ordinary skill in the art at the

time the invention was made to use the register programming of Henry in the control logic circuit of Robbins. One of ordinary skill in the art would have been motivated to use the register programming of Henry in the control logic circuit of Robbins because Henry teaches using the register as a feature control register which configures the functional blocks as enabled or disabled and programming so before shipping; an explicit desire taught by Robbins (column 5, lines 29-31; column 3, lines 44-57).

As per claim 20, Robbins teaches the method of claim 12. Robbins does not explicitly teach wherein the resource status register is implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale. Henry does teach wherein the resource status register is implemented in a programmable read-only memory, and wherein the programmable read-only memory is programmed prior to sale (column 4, lines 57-60).). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the register programming of Henry in the control logic circuit of Robbins. One of ordinary skill in the art would have been motivated to use the register programming of Henry in the control logic circuit of Robbins because Henry teaches using the register as a feature control register which configures the functional blocks as enabled or disabled and programming so before shipping; an explicit desire taught by Robbins (column 5, lines 29-31; column 3, lines 44-57).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: See attached PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher S. McCarthy whose telephone number is (571)272-3651. The examiner can normally be reached on M-F, 9 - 5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571)272-3645. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

csm
April 1, 2005

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100